REMARKS

Applicant would like to thank the Examiner for the consideration given the present application. The Office Action of **February 28, 2001**, has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a Two (2) Month Extension of Time* which extends the shortened statutory period for response to **July 28, 2001 (Saturday)**. Accordingly, Applicant respectfully submits that this response is timely filed.

Claims 1-76 were pending in the present application prior to the aforementioned amendment. By this Amendment, claims 1, 10, 19, 32, 45 and 68 have been amended. Applicant submits that no issue of new matter has been set forth by this Amendment. Accordingly, claims 1-76 are still pending in the subject application and are believed to be in condition for allowance at least for the reasons advanced hereinbelow.

Initially, the Office Action objects to the drawings as containing various informalities. In response thereto, Applicants file concurrently herewith a *Request for Approval of Drawing Changes* to designate Figs. 1 and 2 as "Prior Art," as suggested by the Examiner.

The Official Action next objects to the drawings for including duplicate reference numerals 37 and 39. In response, the drawings and specification are amendment to refer to the contact holes as reference 39b and the interlayer insulating film as reference 37c. It is respectfully submitted that the objection under 1.84(p)(4) is overcome and reconsideration is requested.

Finally, with respect to the drawings, the Official Action objects to the drawings as not showing every feature of the present invention. Specifically, the Official Action asserts that the first and second substrate must be shown or canceled from the claims. Applicant respectfully traverses this, contending that the first and second substrates are shown at least in Fig. 2 as reference numerals 11 and 11' respectively. Reconsideration and withdrawal of the objection is respectfully requested.

Claims 4 and 71 have been objected to for containing an obvious informality. In response thereto, claims 4 and 71 have been amended to correct this informality. Reconsideration and withdrawal of the objection is respectfully requested.

The Office Action rejects claims 1-76 pursuant to 35 U.S.C. §103(a) as unpatentable over ***Sumiyoshi et al. '134A*** in view of ***Ohmura '937***. Applicant respectfully traverses the grounds for rejection at least for the following reasons.

Three criteria must be met to establish a *prima facie* case of obviousness. *M.P.E.P.* §2143. First, there must be some teaching, suggestion, or motivation to combine or modify the teachings of the prior art to produce the claimed invention, found either in the references themselves or in the knowledge generally available to a skilled artisan. *In re Fine*, 837 F.2d 1071, 5 USPQ.2d 1596 (Fed. Cir. 1988). Second, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). And third, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

As amended, the claimed invention is directed generally to a semiconductor device including a thin film transistor comprising a polycrystalline semiconductor layer having source, drain and channel regions; a gate insulating layer adjacent to said channel region; and a gate electrode adjacent to said channel region; an interlayer insulating film comprising an inorganic material formed on said thin film transistor; and an organic resin film provided over said interlayer insulating film; wherein said polycrystalline semiconductor layer exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon to the lower frequency direction.

Applicant respectfully contends that a *prima facie* case of obviousness has not been set forth in the Office Action. In particular, it is contended that the proposed ***Sumiyoshi et al. '134A-Ohmura '937*** combination fails to teach every claimed feature necessary to render the claimed invention obvious under §103. For instance, the Examiner contends that ***Ohmura '937*** discloses a crystalline silicon layer displaced to a lower frequency direction (518 cm^{-1}). However, it appears that the Raman peak in ***Ohmura '937*** should be applied to single crystalline silicon (Column 4, line 43). On the other hand, the claimed invention recites at least claims 1, 19 and 45 that the Raman peak is displaced from the peak of single crystalline silicon. Moreover, the claimed invention is directed to a semiconductor device comprising a polycrystalline semiconductor layer. Such features are not expressly taught or inherently suggested in the proposed ***Sumiyoshi et al. '134A-Ohmura '937*** combination.

Since the proposed ***Sumiyoshi et al. '134A-Ohmura '937*** combination fails to teach every claimed feature of the present invention, it is contended that the claimed invention is patentably distinct over the prior art of record. Reconsideration and withdrawal of the rejection is earnestly solicited.

Accordingly, Applicant respectfully contends that the claimed invention is directed to subject matter which is patentably distinct over the prior art and also submit that the pending claims are in proper condition for allowance and reconsideration and withdrawal of the pending rejection is requested. If the Examiner believes further discussions with Applicants representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,

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IN THE SPECIFICATION

Replace page 17, paragraph 1 with the following:

After removing photoresist 27, the channel regions are then thermally annealed at 600°C for 10 to 50 hours in H_2 atmosphere to make active the impurities in the drain and source regions. An interlayer insulating film 37c of silicon oxide is deposited to a thickness of 0.2 to 0.6 μm by the same sputtering method as described above over the entire surface of the structure followed by etching by means of a photomask ⑤ for opening contact holes 39b through the interlayer film 37c and the oxide film 35 in order to provide accesses to the underlying source and drain regions 34b, 34a, 34b' and 34a'. The deposition of the interlayer insulating film 37c may be carried out by LPCVD, photo-CVD, ordinal pressure CVD (TEOS-ozone) . Next, an aluminum film of 0.5 to 1 μm thickness is deposited on the structure over the contact holes 39b and patterned to form source and drain electrodes 36b, 36a, 36b' and 36a' by means of a photomask ⑥ as illustrated in Fig.8 (F). An organic resin film 39 such as a transparent polyimide film is coated over the structure to provide a planar surface and patterned by means of a photomask ⑦ to provide accesses to the source electrodes 36b and 36b' followed by formation of lead electrode 37 made of a transparent conductive material such as indium tin oxide (ITO) to be electrically connected with the pad 37b. The ITO film is deposited by sputtering at room temperature to 150°C followed by annealing in an oxidizing atmosphere (O_2) or in air at 200 to 400°C. The pad 37b can be formed at the same time by the deposition of the lead electrode 37. Then, the formation of CMOS transistors is finished. The mobility, the threshold voltage of the p-channel TFT are 20 cm^2/Vs and -5.9 V. The mobility, the threshold voltage of the n-channel TFT are 40 cm^2/Vs and 5.0 V. The glass substrate thus provided with these CMOS transistors and suitable conductive patterns as illustrated is joined with a counterpart glass substrate provided with a ground electrode at its entire inner surface followed by injection of a liquid crystal material between the two substrates. One of the advantages of the above process is that the formation of these transistors (spoiled and not spoiled) can be carried out at temperatures no higher than 700°C so that the process does not require the use of expensive substrates such as quartz substrates and therefore suitable for large scale liquid crystal displays production methods.

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IN THE CLAIMS:

1. (Twice Amended) [An electro-optical] A semiconductor device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor having a polycrystalline semiconductor layer comprising source, drain and channel regions;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor;

an organic resin film provided over [said thin film transistor and] said interlayer insulating film; and

a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film,

[wherein said interlayer insulating film is located between said organic resin film and said channel region of the thin film transistor, and]

wherein said [thin film transistor comprises silicon and] polycrystalline semiconductor layer exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon to the lower frequency direction.

4. (Amended) A device according to claim 1 wherein said channel region comprises a material selected [form] from the group consisting of silicon, germanium and a combination thereof.

10. (Twice Amended) [An electro-optical] A semiconductor device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor having a polycrystalline semiconductor layer comprising source, drain and channel regions;

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an interlayer insulating film comprising an inorganic material formed on said thin film transistor;

an organic resin film provided over [said thin film transistor and] said interlayer insulating film; and

a pixel electrode formed over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film,

[wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor,]

wherein said [thin film transistor comprises silicon and] polycrystalline semiconductor layer exhibits a peak of Raman spectra, displaced from 522 cm^{-1} to the lower frequency direction[.], and

wherein said polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer.

19. (Twice Amended) [An electro-optical] A semiconductor device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising:

a polycrystalline [crystalline] semiconductor layer having source, drain and channel regions;

a gate insulating layer adjacent to said channel region; and

a gate electrode adjacent to said channel region;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over [said thin film transistor and] said interlayer insulating film;

[wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor,]

wherein said [thin film transistor comprises silicon and] polycrystalline

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semiconductor layer exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon to the lower frequency direction.

32. (Twice Amended) [An electro-optical] A semiconductor device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising:

a polycrystalline [crystalline] semiconductor layer having source, drain and channel regions;

a gate insulating layer adjacent to said channel region;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over said thin film transistor and said interlayer insulating film;

[wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor, and]

wherein said polycrystalline semiconductor layer comprises silicon and exhibits a peak of Raman spectra, displaced from 522 cm^{-1} to the lower frequency direction[.], and

wherein said polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer.

45. (Twice Amended) [An electro-optical] A semiconductor device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least an n-channel thin film transistor and at least a p-channel thin film transistor both formed over said first substrate, each of said n-channel and p-channel thin film transistors comprising:

a polycrystalline [crystalline] semiconductor layer having source, drain and channel regions;

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a gate insulating layer adjacent to said channel region; and

a gate electrode adjacent to said channel region;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over [said thin film transistor and] said interlayer insulating film;

[wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor,]

wherein said [thin film transistor comprises silicon and] polycrystalline semiconductor layer exhibits a peak of Raman spectra, displaced from a peak of single crystalline silicon to the lower frequency direction.

68. (Amended) [An electro-optical] A semiconductor device comprising:

a first substrate having an insulating surface;

a second substrate opposing said first substrate;

at least one thin film transistor formed on said insulating surface, said thin film transistor comprising:

a polycrystalline [crystalline] semiconductor layer having source, drain and channel regions;

an interlayer insulating film comprising an inorganic material formed on said thin film transistor; and

an organic resin film provided over [said thin film transistor and] said interlayer insulating film;

a pixel electrode provided over said organic resin film and connected to said thin film transistor through an opening provided in said organic resin film;

[wherein said interlayer insulating film is located between said organic resin film and at least said channel region of the thin film transistor, and]

wherein said [channel region comprises silicon and] polycrystalline semiconductor layer exhibits a peak of Raman spectra, displaced from 522 cm^{-1} to the lower frequency direction[.], and

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wherein said polycrystalline semiconductor layer is formed by crystallizing an amorphous semiconductor layer.

71. (Amended) A device according to claim 68 wherein said channel region comprises a material selected [form] from the group consisting of silicon, germanium and a combination thereof.